REMARKS

I. Rejections Under 35 U.S.C. § 103(a)

Claims 1-28 were previously cancelled and claims 29-39 previously submitted in Paper No. 7, which constituted an amendment provided as submission under 37 C.F.R. § 1.114. No amendments to the claims are presented herein. Claims 29-39 were rejected by the Examiner in Paper No. 9 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,016,000 to Moslehi in view of U.S. Patent No. 6,417,088 to Ho et al ("Ho").

Regarding claim 29, the Examiner argued that Moslehi discloses a method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit (IC) device comprising the steps of: providing a substrate, Fig. 15, thereafter configuring substrate to comprise a wiring bond pad to comprise a single metal layer, step 144, Fig. 6B, wherein the single metal layer does not share a single metal layer with any other material, thereafter positioning at least one IC device below the wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer, column 1, lines 10-25, thereafter locating the single metal layer above a plurality of intermetal dielectric (IMD) layers, steps 122, Fig. 6B, and thereafter locating at least one IC device below the plurality of IMD layers, FIG. 15, wherein the single metal layer comprises a metal-8 layer.

The Examiner admitted that Moslehi does not expressly disclose locating a buffer and bonding layer immediately above a single metal layer. The Examiner argued, however, that Ho discloses a method for forming a wiring bond pad 30, column, 3, line 10, comprising an aluminum buffer layer 52, Fig. 6, column 4, lines

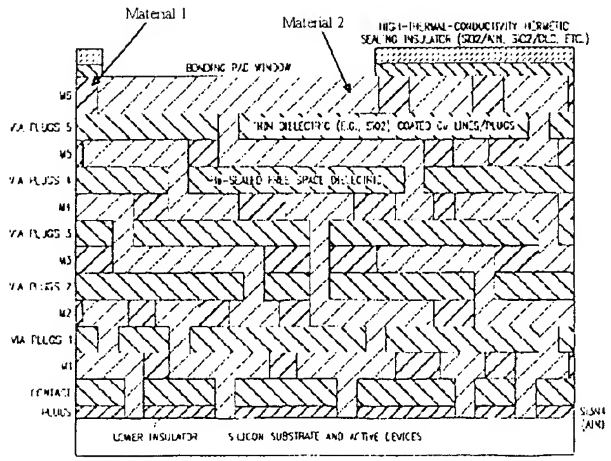
1 and bonding layer 60, column 4, line 53, immediately above single metal layer 30. The Examiner argued that at the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the buffer layer and bonding layer teaching of Ho and Moslehi, because it would have increased the adhesion between the bond pad and the bonding layer as taught by Ho, column, 4, lines 30-32.

The Applicants respectfully disagree with this assessment. Applicants' claim 29 is directed toward a method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit device, said method comprising the steps of: providing a substrate; thereafter configuring said substrate to comprise a wiring bond pad to comprise a single metal layer, wherein said single metal layer does not share said single metal layer with any other material; thereafter positioning at least one integrated circuit device below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad to comprise a single metal layer; thereafter locating a buffer and bonding layer immediately above said single metal layer; thereafter locating said single metal layer above a plurality of intermetal dielectric layers; and thereafter locating said at least one integrated circuit device below said plurality of intermetal dielectric layers, wherein said single metal layer comprises a metal-8 layer.

The Examiner also argued that step 122, Fig. 6B, of Moslehi teaches "thereafter locating the single metal layer above a plurality of intermetal dielectric (IMD) layers". This is also not the case. Step 122 of Moslehi refers to "deposit multi-layer disposable dielectric stack...." This stack is not an IMD layer. Additionally, such a stack is not a plurality of IMD layers. Also, Applicants step of

"thereafter locating said single metal layer above a plurality of intermetal dielectric layers" occurs AFTER the step of "thereafter positioning at least one integrated circuit device below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad to comprise a single metal layer; thereafter locating a buffer and bonding layer immediately above said single metal layer". This sequence of process steps is not taught or suggested by Moslehi. The Examiner has not indicated that the sequence of steps of Moslehi teaches or suggests the SAME sequence of steps of Applicants' claim 29.

Additionally, FIG. 15 of Moslehi does NOT teach a single metal layer comprising a metal-8 layer as the Examiner suggests. In fact FIG. 15 of Moslehi only shows M1 to M6 layers. The Applicants also point out that FIG. 15 does not show any "single layers" which are made up of only one material. Each layer of FIG. 15 shares one type of material with another type of material within the same layer. FIG. 15 is reproduced below to point out to the Examiner that FIG. 15 does not show a single metal layer that is made up of only that type of material. For example, the M6 layer is comprised of more than one type of material – material 1 and material 2. This is also true of all of the other layers of FIG. 15



It is clear that FIG. 15 of Moslehi simply does NOT show a single metal layer does not share the same single metal layer with any other material, and wherein at least one integrated circuit device is thereafter positioned below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad to comprise a single metal layer. Additionally, Moslehi does not show a buffer and bonding layer immediately above said single metal layer.

Additionally, column 1, lines 10-25 of Moslehi does not teach "...wherein the single metal layer does not share a single metal layer with any other material, thereafter positioning at least one IC device below the wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer." Instead, col. 1, lines 10-25 of Moslehi is directed toward an ultra high-speed chip interconnect structure and methods of forming such a structure that integrates free-space intermetal and

interlevel dielectric regions with at least one high conductivity interconnect conduct for the purpose of establishing optimally low permittivity between adjacent interlevel and interlevel conductor lines and plugs, etc.

Col. 1, lines 10-25 of Moslehi does NOT indicate the steps of thereafter positioning at least one integrated circuit device below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad to comprise a single metal layer; and thereafter locating a buffer and bonding layer immediately above said single metal layer. Again, the sequence of steps is an important feature of Applicants' claim 29. The Applicants ask the Examiner to consider that the word "thereafter" as utilized in Applicants' claim 29 is important because Moslehi does not show this particular sequence. Additionally, Moslehi does not indicate that wiring bond pad efficiency can be improved as a result of configuring said wiring bond pad to comprise a single metal layer.

The Examiner asserted that step 144 of FIG. 6B of Moslehi shows a wiring bond pad to comprise a single metal layer. This is not the case. Step 144 of Moslehi refers to "microlithography pattering and formation of bonding pad windows by dielectric RIE". Further , as indicated col. 16, lines 50-64 of Moslehi, an etch-back process with respect to step 144 is described, but no suggestion or teaching of a wiring bond pad comprising a single metal layer" is disclosed by Moslehi. Additionally, Applicants' claim 29 indicates that the single metal layer does not share said single metal layer with any other material. Moslehi does not indicate that a single metal layer does not share the same metal layer with any other material. The Examiner has not adequately cited a portion or Figure of Moslehi, which teaches or suggests that the single metal layer does not share the same

metal layer with any other materials. The Examiner cited column 1, lines 10-25 of Moslehi, but again, this cited section does not teach a single metal later which does not share the same metal layer with any other materials.

The Examiner argued that Ho discloses a method for forming a wiring bond pad 30, column, 3, line 10, comprising an aluminum buffer layer 52, Fig. 6, column 4, lines 1 and bonding layer 60, column 4, line 53, immediately above single metal layer 30. Again, Ho does not teach or suggest a wiring bond pad comprising a single metal layer, wherein said single metal layer does not share said single metal layer with any other material. Applicants refer the Examiner to a copy of FIG. 6 below, and a mark-up thereof, which indicates that FIG. 6 shows at least two different types of materials located on the same single layer. Additionally, neither Ho nor Moslehi teach a single layer composed only of a metal-8 layer. Thus, because neither Ho nor Moslehi teach a wiring bond pad comprising a single metal layer, wherein said single metal layer does not share said single metal layer with any other material, Ho and Moslehi cannot properly be combined within one another as a basis for rejection claim 29 under 35 U.S.C. 103 (a).

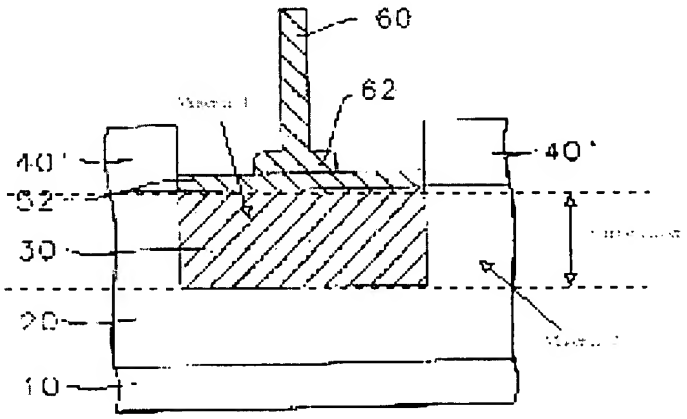


FIG. 6

Regarding claims 30-31, the Examiner argued that Moslehi discloses a method wherein the plurality of IMD layers comprises at least IMD-1 to IMD-7 layers, Fig. 15, and step 132, Fig. 6B, wherein the metal-8 layers comprise a copper layer, step 130, Fig. 6B. The Applicants respectfully disagree with this assessment. Step 132 of Fig. 6B only asks whether additional interconnect levels are required, but does not mention specific IMD-1 to IMD-7 layers. Additional, step 130 refers only to copper CMP to form embedded inlaid metal lines, but does not refer specifically to IMD-1 to IMD-7 layers, nor even a metal-8 layer, and in particular a single metal layer made of only type of material. Again, neither Moslehi nor Ho teach a single metal layer that is made up of only one type of material (i.e., which does not share the same layer with another type of material). Thus, the rejection to claims 30-31 should be withdrawn.

Regarding claims 32, 38-39, the Examiner argued that Moslehi discloses a method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit (IC) device comprising the steps of: providing a substrate, Fig. 15, thereafter configuring the substrate to comprise a wiring bond pad to comprise a single metal layer, step 144, Fig. 6B, wherein a single metal layer does not share a single metal layer with any other material, thereafter locating at least one IC device below the wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer, column 1, lines 10-25, thereafter locating a single metal layer above a plurality of IMD layers, wherein a plurality of IMD layers comprises at least IMD-1 to IMD-7, Fig. 15, and step 132, Fig. 6B, and thereafter locating at least one IC device below the plurality of IMD layers, Fig. 15, wherein a single metal layer comprises a metal-8 of copper, step 130, Fig. 6B. Again, neither Moslehi nor Ho teach a single

metal layer that is made up of only one type of material (i.e., which does not share the same layer with another type of material). Thus, the rejection to claims 30-31 should be withdrawn.

The Examiner admitted that Moslehi does not expressly disclose locating a buffer and bonding layer immediately above the single metal layer comprises a layer having a thickness in a range of and including 10KÅ to 20KÅ. The Examiner argued, however, that Ho discloses the method for forming a wiring bond pad 30, column 3, lines 10, comprising an aluminum buffer layer 52, Fig. 6, column 4, line 1, and a bonding layer 60, column 4, line 53, immediately above single metal layer 30. The Examiner stated that at the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the buffer layer and bonding layer teaching of Ho with Moslehi, because it would have increased the adhesion between the bond pad and the bonding layer as taught by Ho, column 4, lines 30-32.

With respect to the thickness, the Examiner argued that Ho discloses the method for forming a wiring bond pad, Fig. 6, comprising an aluminum buffer layer 52, column 3, line 3, and bonding layer 60, column 4, line 53, immediately above metal layer 30, wherein the aluminum buffer layer has a thickness in range of 5000Å, column 4, line 35. The Examiner therefore argued that it would have been obvious to one of ordinary skill in the art to use the buffer layer 52 teaching of Ho in the range as claimed, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover optimum or workable range by routine experimentation.

The Applicants respectfully disagree with this assessment. Step 144, Fig. 6B of Moslehi does not show a single metal layer that does not share a single metal layer with any other material. Step 144 only refers to microlithography patterning and formation of bonding pad windows by electric die but dose not suggest or teach a single metal layer that does not share a single metal layer with any other material, particularly one related to a bonding pad. Additionally, as explained previously, column 1, lines 10-25 does not refer to locating at least one IC device below the wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer. Moslehi simply does not teach a single metal layer which does not share the same layer space with another material. The Applicants refer the Examiner again to FIG. 15 of Moslehi, which is reproduced herein above for evidence of the lack of such a single metal layer thereof. Thus, column 1, lines 10-25 does not refer to any efficiency for a bonding pad that can be achieved through implementing the processes of Applicants' claims 32, 38-39.

Regarding claims 33-37, the Examiner admitted that Moslehi does not disclose the single metal layer comprising a copper layer having a thickness of approximately 10-18KÅ. The Examiner argued, however, that Moslehi discloses the copper single metal layer formed with a thinner thickness, column 2, lines 7-15, and line 31. The Examiner therefore argued that it would have been obvious to one of ordinary skill in the art to use the teaching of Moslehi in the range as claimed, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover optimum or workable range by routine experimentation. The Applicants respectfully disagree with this assessment.

Applicants' claim 33 is directed toward a copper layer (i.e., single metal layer) having a thickness of approximately 10KÅ. Applicants' claim 34 is directed toward a copper layer (i.e., single metal layer) having a thickness of approximately 12KÅ. Applicants' claim 35 is directed toward a copper layer (i.e., single metal layer) having a thickness of approximately 14KÅ. Applicants' claim 36 is directed toward a copper layer (i.e., single metal layer) having a thickness of approximately 16KÅ. Applicants' claim 37 is directed toward a copper layer (i.e., single metal layer) having a thickness of approximately 18KÅ. As explained above, neither Moslehi nor Ho teaches a single metal layer composed of just that...the same material or metal. In claims 33-37, copper is used as the only material for forming a single metal layer. Both Ho and Moslehi teach the opposite, which are multiple layers wherein each layer is composed of more than one type of material.

Thus, both Ho and Moslehi teach away from a single metal layer formed from only one material. Thus, the general conditions of the claims were not disclosed in the prior art because the prior art (i.e., Moslehi and/or Ho) do not teach either separately or in combination with one another the single metal layer as described herein. Thus, the thickness values disclosed above of the copper layer of Applicants' claims 33-37 do comprise an inventive step, which must be considered by the Examiner in light of the fact that Moslehi and/or Ho fail to teach a single metal layer that does not share the same layer with any other material and one which is particularly associated with a bonding pad.

The Applicants also point out to the Examiner that the Ho reference was issued on July 9, 2002, while Applicants' patent application was filed on January 9, 2002. Thus, because the Ho reference issued after Applicants' invention was filed, it is not clear that the Ho reference constitutes prior art for purposes of a rejection

under 35 U.S.C. 103(a). In such a case, the Ho reference cannot properly combined with another reference such as Moslehi as a basis for a rejection to claims 29-39 under 35 U.S.C. 103(a).

Additionally, the Examiner has not provided a motivation for combining Ho with Moslehi as a basis for rejecting Applicants' claims 29-39. Why would one skilled in the art have been motivated to combine two references that each does not teach a single metal layer that does not share the same layer with another material? Additionally, why would one skilled in the art have been motivated to have combined a reference (Ho), which did not even issue until after the Applicants' invention was filed. Such a motivation must be provided in order to assert a rejection under 35 U.S.C. 103(a).

The Applicants remind the Examiner that the language of the references may not taken out of context and combined them without motivation, in effect producing the words of the claims (and sometimes, not even the words or concepts of the claims), without their meaning or context. The resultant combination would not yield the invention as claimed. The claims are rejected under 35 U.S.C. §103(a) and no showing has been made to provide the motivation as to why one of skill in the art would be motivated to make such a combination, and further fails to provide the teachings necessary to fill the gaps in these references in order to yield the invention as claimed.

The rejections under 35 U.S.C. §103(a) have provided no more motivation than to simply point out the individual words of the Applicant's claims among the references, but without the reason and result as provided in the Applicant's claims and specification, and without reason as to why and how the references could

provide the Applicant's invention as claimed. Hindsight cannot be the basis for motivation, which is not sufficient to meet the burden of sustaining a 35 U.S.C. §103(a) rejection.

Thus, claims 29-39 of the present invention are not taught or suggested by Ho and/or Moslehi. Combining these references fails to teach or yield the invention as claimed. The combination of these references fails to teach or suggest all the elements of the claims. Further, one of skill in the art would not be motivated to make such a combination. Therefore, the present invention is not obvious in light of any combination of Ho and/or Moslehi. Withdrawal of the §103(a) rejection is therefore respectfully requested.

II. Conclusion

In view of the foregoing discussion, Applicants have responded to each and every rejection of the Official Action, and respectfully request that a timely Notice of Allowance be issued. Applicants have clarified the structural distinctions of the present invention. Applicants respectfully submit that the foregoing discussion does not present new issues for consideration and that no new search is necessitated. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections under 35 U.S.C. 103(a) , and further examination of the present application.

Should there be any outstanding matters that need to be resolved in the present application; the Examiner is respectfully requested to contact the undersigned representative to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,

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